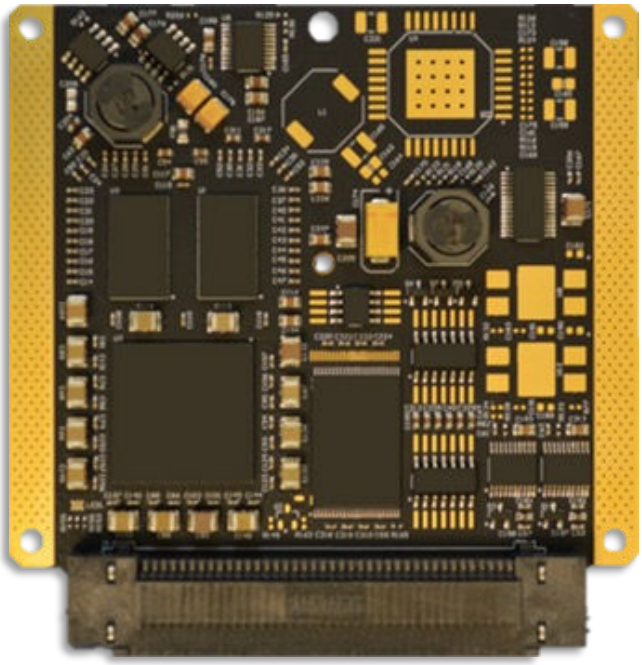
CSP

OVERVIEW

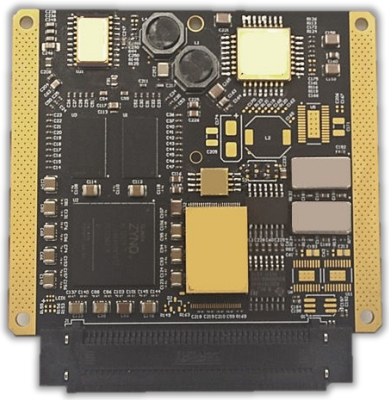
Compact Space Processor (**CSP**) is a re-envisioned, upgraded version of the CSPv1 design, inititally developed in collaboration with NASA GSFC and NSF CHREC. CSP is a high-performance compact form-factor design featuring the AMD-Xilinx Zynq-7020 System-on-Chip (SoC). This design has supported numerous science and defense missions and has led to several spin-off designs and advanced research concepts.



CSP EM

KEY FEATURES

- Compact Single Board Computer designed around AMD-Xilinx Zynq-7020 SoC
- High-Heritage, TRL-9, enabled multiple missions
- Radiation mitigation coupled with extensive academic publications
- Inspired NASA-supported equivalent mission-specific designs
- 1U small form-factor (8.81 cm × 8.95 cm)
- Robust hybrid computing platform for wide range of applications
- Low size, weight, power, and cost (SWaP-C)

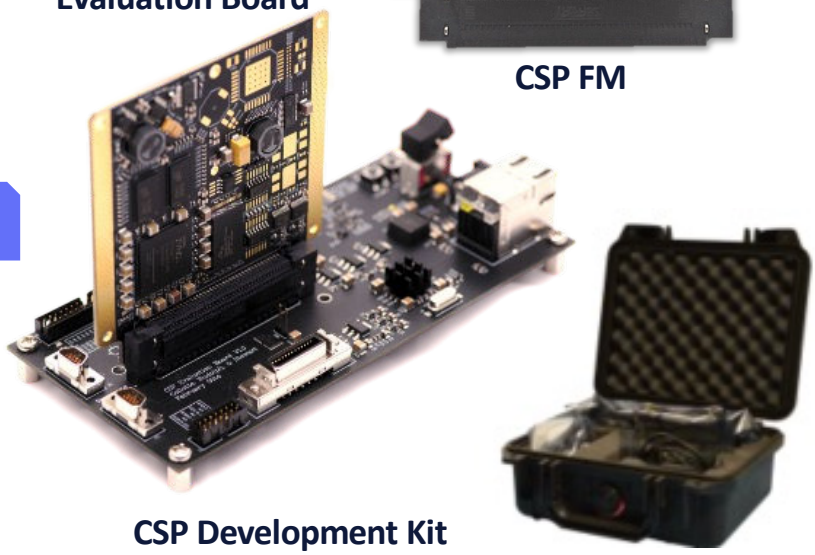


CSP FM

CSP EM in Active Evaluation Board

APPLICATIONS

- Earth Observation
- Small Sat Processor
- Constellation Cluster Computing
- Instrument Payload Backend Processor



CSP Development Kit

CSP

PRODUCT SPECIFICATIONS

AMD-Xilinx Zynq 7020 SoC	
Processing System (PS)	**Dual-Core ARM Cortex-A9** • Up to 667 MHz (-1) / 766 MHz (-2) • 32KB I/D L1 Caches per core and 512KB Unified L2 Cache • NEON SIMD Engine and Single/Double-Precision Vector FPU per core
Programmable Logic (PL)	**Artix 7-Series FPGA** • 53.2K Look-Up Tables (LUTs) • 4.9 Mb Block RAM • 220 DSP Slices • 12-bit XADC (monitor on-chip temperature and VCC)
Memory / Storage	
Volatile Memory	Up to 1 GB (two 512 MB DDR3 SDRAM components) with ECC
Nonvolatile Storage	32 Gb Rad-Tolerant NAND Flash (FM) or 8 Gb NAND Flash (EM)
Supported Interfaces	
Backplane Connectivity	12× Single-Ended I/O at 1.8V, 2.5V, or 3.3V 24× LVDS pairs (48× Single-Ended I/O at 1.8V, 2.5V, or 3.3V)
PS MIO Interfaces	RGMII for 10/100/1000 Ethernet* ULPI for USB 2.0 OTG* CAN 2.0B (1 Mbps)* SPI (3 chip selects) I2C (external 3.3V pull-ups required) UART (max baud rate of 921600)
Additional Details	
Software / FPGA	Space Micro Reference Design for SSP with Active Evaluation Board (e.g., PetaLinux and NASA cFS, with COSMOS v5+ Integration)
Fault Tolerance	Onboard watchdog timer, ECC DDR3 memory, redundant boot image storage, etc.
Radiation Performance	TID 30+ krads(Si) No SEL susceptibility up to 42 MeV·cm^2·mg^{-1} SEU rate of 0.10 SEUs/device/day in LEO or 0.82 SEUs/device/day in GEO
Power	1.6 – 3.6 Watts (FPGA Load dependent)
Operating Temperature	–35 to +85 °C (FM) or ±0 to +70 °C (EM)
Mechanical	1U CubeSat form factor (NASA CS^2 Compliant) FM ~82g, 620 mil thick
Active Evaluation Board	
Interfaces and Functionality	10/100/1000 Ethernet (RJ45) USB 2.0 OTG (USB Type-A) JTAG and UART through FTDI USB-to-UART/MPSSE Converter (USB Micro-B) 12-pin PMOD Header Reset Control and Power Monitoring FMC†

*External PHY required

†Partial subset of LPC

*Subject to change without notice