SSP

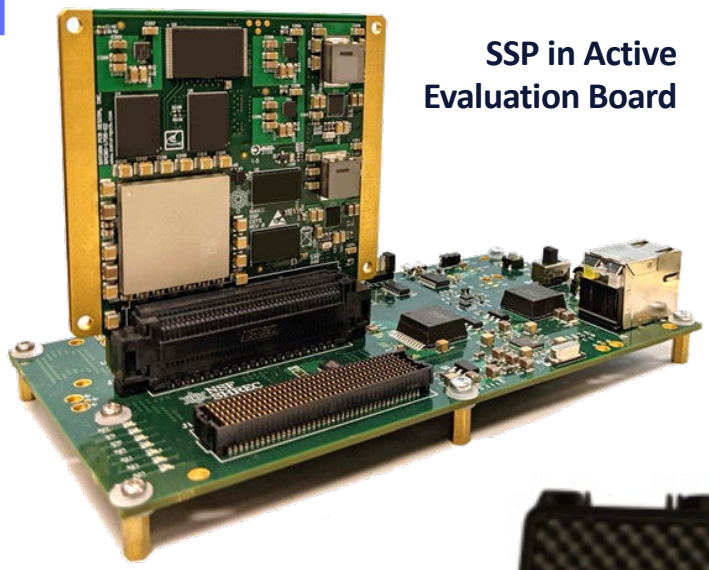
OVERVIEW

Space Systems Processor (SSP) is the successor to the CSP. It is re-envisioned to build on the CSPv1 design that was collaboratively developed between NASA GSFC and NSF CHREC. SSP is a high-performance compact form-factor design featuring the AMD-Xilinx Zynq-7045 System-on-Chip (SoC) with additional memory, I/O, and multi-gigabit transceivers for advanced data processing. This design has been proposed on multiple science and defense missions and serves as an ideal platform for high-speed instrument and sensor interfaces.

SSP

KEY FEATURES

- Compact Single Board Computer designed around AMD-Xilinx Zynq-7045 SoC
- High-Heritage, TRL-9
- Radiation mitigation techniques and multiple academic references
- Inspired NASA-supported equivalent mission-specific designs
- 1U small form-factor (8.81 cm × 8.95 cm)
- Robust hybrid computing platform for wide range of applications
- Low size, weight, power, and cost (SWaP-C)



SSP in Active Evaluation Board

APPLICATIONS

- Earth Observation
- Small Sat Processor
- Constellation Cluster Computing
- Instrument Payload Backend Processor

SSP Development Kit

SSP

PRODUCT SPECIFICATIONS

AMD-Xilinx Zynq 7045 SoC	
Processing System (PS)	**Dual-Core ARM Cortex-A9** • Up to 667 MHz (-1) / 800 MHz (-2) • 32KB I/D L1 Caches per core and 512KB Unified L2 Cache • NEON SIMD Engine and Single/Double-Precision Vector FPU per core
Programmable Logic (PL)	**Kintex 7-Series FPGA** • 218.6 K Look-Up Tables (LUTs) • 19.2 Mb Block RAM • 900 DSP Slices • 8 GTX Transceivers (supports up to PCIe 2.0 ×8) • 12-bit House Keeping ADC to monitor voltages, currents, and temperatures
Memory / Storage	
Volatile Memory	Separate 1 GB DDR3 SDRAM Interfaces with ECC for PS and PL
Nonvolatile Storage	32 Gb Rad-Tolerant NAND Flash
Supported Interfaces	
Backplane Connectivity	48× Single-Ended I/O at 1.8V or 3.3V 36× LVDS Pairs (72x Single-Ended I/O at 1.8V, 2.5V, or 3.3V) 8× GTX transceivers (up to 12.5 Gbps per lane)
PS MIO Interfaces	RGMII for 10/100/1000 Ethernet* ULPI for USB 2.0 OTG* CAN 2.0B (1 Mbps)* SPI (3 chip selects) I2C (external 3.3V pull-ups required) UART (max baud rate of 921600)
Additional Details	
Software / FPGA	Space Micro Reference Design for CSP with Active Evaluation Board (e.g., PetaLinux and NASA cFS, with COSMOS v5+ Integration)
Fault Tolerance	Onboard watchdog timer, ECC DDR3 memory, redundant boot image storage, etc.
Radiation Performance	TID 20 krads(Si) No SEL susceptibility up to 42 MeV·cm^2·mg^{-1} SEU rate of 0.92 SEUs/device/day in LEO or 3.24 SEUs/device/day in GEO
Power	2.6 – 15.5 Watts (FPGA Load dependent) on Single 5V Supply
Operating Temperature	–35 to +85 °C (Derated)
Mechanical	3.475 × 3.490 × 0.735 in^3 (1U) (NASA CS^2 Compliant) at 140 grams
Active Evaluation Board	
Interfaces and Functionality	10/100/1000 Ethernet (RJ45) USB 2.0 (USB Type-A) JTAG and UART through FTDI USB-to-UART/MPSSE Converter (USB Micro-B) 12-pin PMOD Header Reset Control and Power Monitoring FMC (34 Differential Pairs + 8 GTX Lanes)

*External PHY required

*Subject to change without notice