VOYAGER

SPACE EDGE™

# A1 SINGLE - BOARD COMPUTER

The Voyager FPGA + LX2160 Orbital Processor (A1) architecture is an advanced, radiation-tolerant 3U SOSA-aligned single-board computer featuring a Teledyne LX2160A processor coupled with an AMD Kintex Ultrascale KU115 FPGA. Both devices are supported by a rad-hard monitor (RHM) which provides reliable boot, configuration, and scrubbing support. This architecture provides extreme flexibility and high performance, enabling payload developers with the best of both worlds with multi-core CPUs and massive FPGA fabric.

16-CORE CPU

KU115 FPGA

RAD-TOLERANT

## APPLICATION

- SOSA Aligned 3U VPX Boxes
- Avionics and instrument boxes
- Rapid, fast-turn space missions
- SmallSat missions
- Signal processing workloads for high-performance and parallel processing

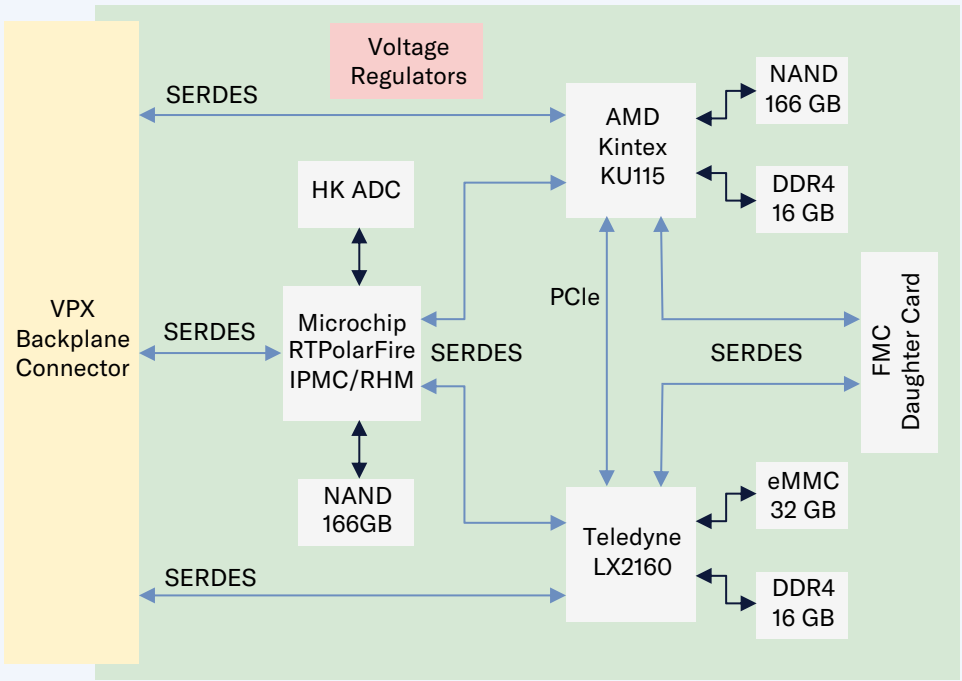


FIGURE 1 | A1 BLOCK DIAGRAM

## KEY FEATURES

1. **SOSA Aligned:** Ensures broad cross-platform interoperability and aligns with DoD MOSA mandates for new acquisitions
2. **Multi-Core Processing:** 16x ARM A72 cores for traditional processing tasks
3. **FPGA Acceleration:** High-performance FPGA fabric for hardware acceleration
4. **Reliable Configuration:** CPU and FGPA monitoring with boot and configuration support via RHM
5. **Real-Time Monitoring :** ADC monitors onboard voltage, temperature, and current
6. **Health Telemetry:** IPMC reports health telemetry information to system manager
7. **Radiation-tolerant design**

# PRODUCT SPECIFICATIONS

| Specifications: SOSA Aligned Single Board Computer | |
|---|---|
| **Processors** | • 16x Arm-Cortex A72 Processors @ 2.2GHz<br>• ~201K DMIPS |
| **Programmable Logic** | • 1,451,000 System Logic Cells<br>• 5,520 DSP Slices<br>• 75.9 Mb BRAM |
| **Memory** | LX2160 CPU:<br>• 16 GB DDR4<br>• 32 GB eMMC<br>KU115 FPGA:<br>• 166GB NAND Flash<br>• 16 GB DDR4 |
| **RHM** | • Housekeeping ADC for monitoring voltage, current, and temperatures<br>• Boot, configuration, and scrubbing support for CPU and FPGA via SelectMAP and PCIe<br>• Board-level power sequencing and control |
| **IPMC** | • Tier 3 system-level capabilities defined under VITA 46.11 |
| **Interface Options** | • FMC expansion cards available for functional expansion<br>• Dedicated debug UART and JTAG for RHM, CPU, and FPGA<br>• Data plane configurations<br>  • ×10 10GBASE-KR or<br>  • ×3 50GBASE-KR2 or<br>  • ×2 100GBASE-KR4 and ×1 50GBASE-KR2<br>• ×4 1000BASE-KX<br>• ×3 PCIe to backplane and ×1 PCIe to FMC<br>• ×3 SpaceWire ports<br>• ×4 GTY lanes to FMC |
| **Form Factor** | • 3U SOSA SpaceVPX<br>• 220-mm Card Length<br>• 1.8-inch Pitch |
| **Estimated Max Power** | • 0.5 W for IPMC<br>• 2.0 W for RHM<br>• 50 – 100W total card power, highly dependent on use case |
| **Radiation Qualification** | • Designed to QML Class P |